

**FIGURE 1**

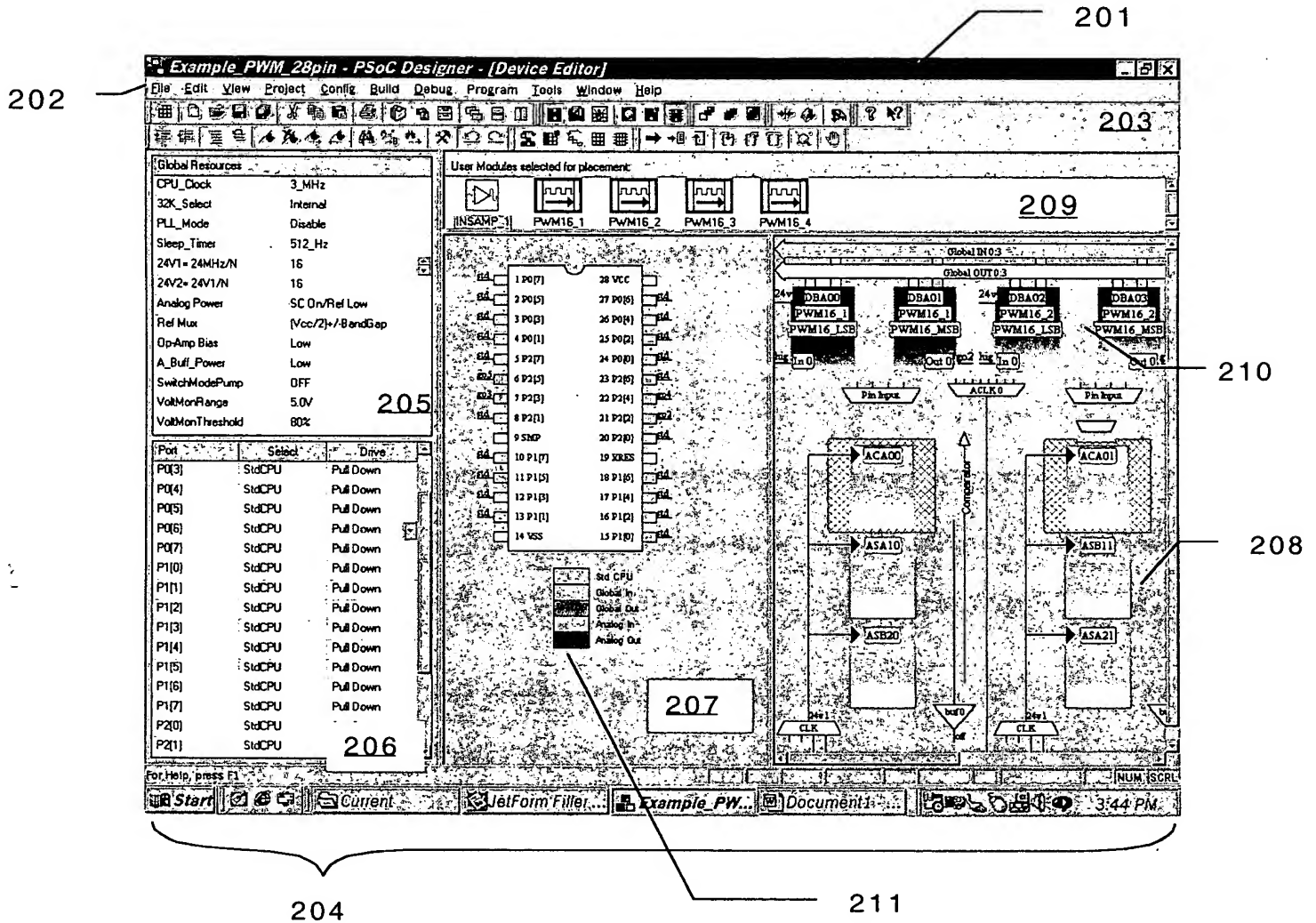


FIGURE 2

**Pin Configuration:**

| Pin Number | Signal Name | Direction / Type |
|------------|-------------|------------------|
| 1          | P0[7]       | STD CPU          |
| 2          | P0[5]       | STD CPU          |
| 3          | P0[3]       | STD CPU          |
| 4          | P0[1]       | STD CPU          |
| 5          | P2[7]       | STD CPU          |
| 6          | P2[5]       | STD CPU          |
| 7          | P2[3]       | STD CPU          |
| 8          | P2[1]       | STD CPU          |
| 9          | SMP         | GLOBAL IN        |
| 10         | P1[7]       | STD CPU          |
| 11         | P1[5]       | STD CPU          |
| 12         | P1[3]       | STD CPU          |
| 13         | P1[1]       | STD CPU          |
| 14         | VSS         | GLOBAL IN        |
| 15         | P1[0]       | STD CPU          |
| 16         | P1[2]       | STD CPU          |
| 17         | P1[4]       | STD CPU          |
| 18         | P1[6]       | STD CPU          |
| 19         | XRES        | GLOBAL IN        |
| 20         | P2[0]       | STD CPU          |
| 21         | P2[2]       | STD CPU          |
| 22         | P2[4]       | STD CPU          |
| 23         | P2[6]       | STD CPU          |
| 24         | P0[0]       | STD CPU          |
| 25         | P0[2]       | STD CPU          |
| 26         | P0[4]       | STD CPU          |
| 27         | P0[6]       | STD CPU          |
| 28         | VCC         | GLOBAL IN        |

**Legend:**

- STD CPU (Diagonal lines)
- GLOBAL IN (Horizontal lines)
- GLOBAL OUT (Cross-hatch)
- ANALOG IN (Dotted)
- ANALOG OUT (Solid black)

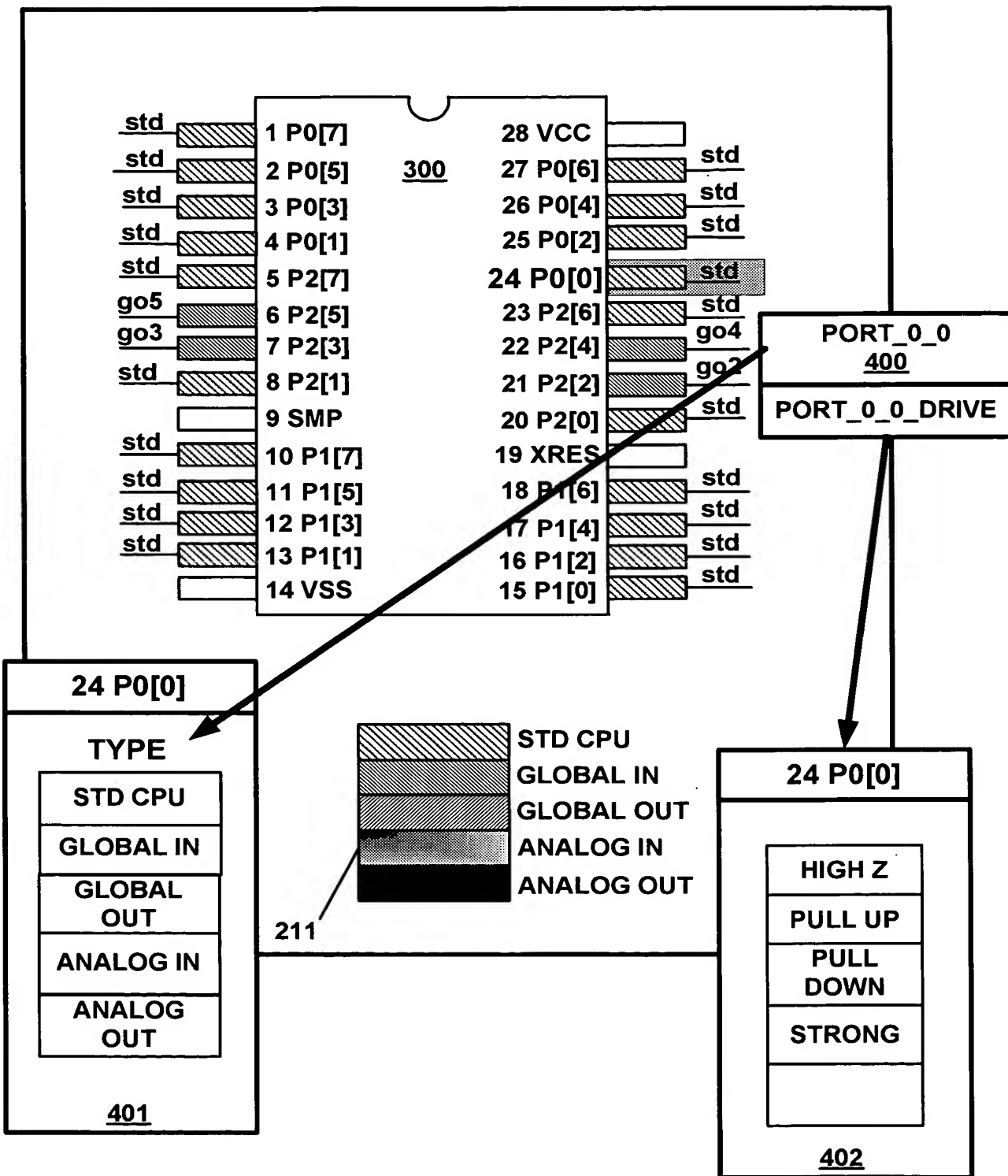


FIGURE 4



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501

| 501    |            |           | 506 |
|--------|------------|-----------|-----|
| PORT   | SELECT     | DRIVE     |     |
| P0 [0] | StdCPU     | HIGH Z    | 505 |
| P0 [1] | StdCPU     | PULL DOWN |     |
| P0 [2] | StdCPU     | PULL DOWN |     |
| P0 [3] | StdCPU     | PULL DOWN |     |
| P0 [4] | StdCPU     | PULL DOWN |     |
| P0 [5] | StdCPU     | PULL DOWN |     |
| P0 [6] | StdCPU     | PULL DOWN |     |
| P0 [7] | StdCPU     | PULL DOWN |     |
| P1 [0] | StdCPU     | PULL DOWN |     |
| P1 [1] | StdCPU     | PULL DOWN |     |
| P1 [2] | StdCPU     | PULL DOWN |     |
| P1 [3] | StdCPU     | PULL DOWN |     |
| P1 [4] | StdCPU     | PULL DOWN |     |
| P1 [5] | StdCPU     | PULL DOWN |     |
| P1 [6] | StdCPU     | PULL DOWN |     |
| P1 [7] | StdCPU     | PULL DOWN |     |
| P2 [0] | StdCPU     | PULL DOWN |     |
| P2 [1] | GLOBAL OUT | PULL DOWN |     |
| P2 [2] | GLOBAL OUT | PULL DOWN |     |
| P2 [3] | GLOBAL OUT | PULL DOWN |     |

502

503

504

506

206

FIGURE 5

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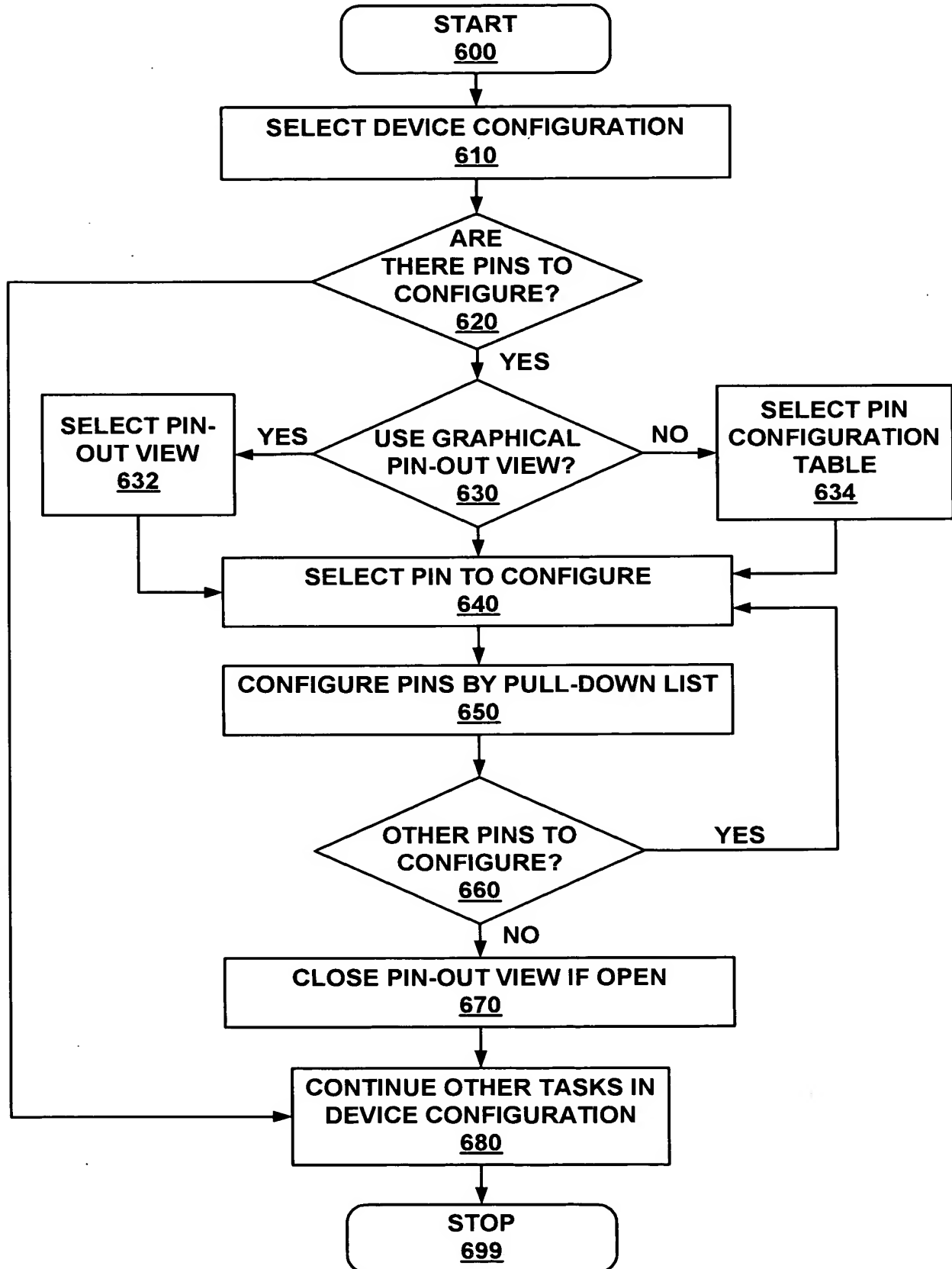


FIGURE 6